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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AKINYEMI, AJIBOLA A	

ART UNIT	PAPER NUMBER
2618	

NOTIFICATION DATE	DELIVERY MODE
07/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/580,645	IIDA, SACHIO	
	Examiner	Art Unit	
	AJIBOLA AKINYEMI	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/25/2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/29/2009 has been entered.

Drawings

2. Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art henceforth "Admission" and further in view of Feld (Patent No.: US 6281755B1).

With respect to claim 9:

Admission discloses an amplifier comprising: an amplification device (fig.8, item 102), an output terminal of the amplification device being an output terminal of the amplifier (fig.8, item 102) and an LC parallel resonant circuit (fig.8, item 103,104) connected in parallel to the amplification device (fig.8, item 102). Admission did not disclose LCR series resonant circuit connected in parallel to the amplification device and the LC parallel resonant circuit. Feld discloses LCR series resonant circuit (fig.5, Ls Cs GL) and the LC parallel resonant circuit (fig. 5). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to have the above limitation of Feld for impedance matching.

6. Claim 10, 1, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art henceforth "Admission" and further in view of Feld (Patent No.: US 6281755B1) and Kaczynski (2007/0111684A1).

With respect to claim 10:

The rejection of claim 9 is incorporated; Admission and Feld did not disclose an amplifier wherein a common gate circuit and a cascade circuit are combined. Kaczynski disclosed an amplifier wherein a common gate circuit and a cascade circuit are combined (parag.0034). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a common gate circuit and cascade circuit combined together in order to amplify the signal.

With respect to claim 11:

The rejection of claim 9 is incorporated; Admission and Feld did not disclose an amplifier wherein a common-source circuit, a cascade circuit and a voltage feedback circuit are combined but the examiner take official action that combining common source circuit, a cascade circuit and a voltage feedback is common in the art and it would have been obvious to one of ordinary skill in the art at the time the invention as made to have this limitation in order to amplify the signal.

With respect to claim 17:

The rejection of claim 14 is incorporated; Admission, Feld and Kasuga did not disclose common gate circuit and a cascade circuit combine together. Kaczynski disclosed an amplifier wherein a common gate circuit and a cascade circuit are combined (parag.0034). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a common gate circuit and cascade circuit combined together in order to amplify the signal.

With respect to claim 18:

The rejection of claim 14 is incorporated; Admission, Feld and Kasuga did not disclose a common source circuit, a cascade and voltage feedback circuit to be combined but the examiner take official action that combining common source circuit, a cascade circuit and a voltage feedback is common in the art and it would have been obvious to one of ordinary skill in the art at the time the invention as made to have this limitation in order to amplify the signal.

7. Claims 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art henceforth "Admission" and further in view of Feld (Patent No.: US 6281755B1) and Shohara (Pub. No.: US 2005/0078743A1).

With respect to claims 12:

Admission discloses an amplifier comprising: an amplification device (fig.8, item 102), an output terminal of the amplification device being an output terminal of the amplifier (fig.8, item 102) and an LC parallel resonant circuit (fig.8, item 103,104) connected in parallel to the amplification device (fig.8, item 102). Admission did not disclose an

antenna, a band pass filter and low noise amplifier, converter, automatic gain control, processor , LCR series resonant circuit. Feld discloses LCR series resonant circuit (fig.5, Ls Cs GL) and the LC parallel resonant circuit (fig. 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the above limitation of Feld for impedance matching. Shohara disclosed a wireless communication apparatus comprising a low noise amplifier configured to amplify a voltage of a received signal (parag. 0034), a down-converter (fig.1, item 14) configured to down-convert the voltage-amplified received signal by frequency conversion, an automatic gain controller (fig.1, item 28), an analog-digital converter (fig.1, item 18), and a signal processing circuit configured to perform digital signal processing of received data (fig.1, item 50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have all this limitation for a design choice.

With respect to claim 13:

Admission discloses an amplifier comprising: an amplification device (fig.8, item 102), an output terminal of the amplification device being an output terminal of the amplifier (fig.8, item 102) and an LC parallel resonant circuit (fig.8, item 103,104) connected in parallel to the amplification device (fig.8, item 102). Admission did not disclose an antenna, a band pass filter and low noise amplifier, converter, automatic gain control, processor and LCR series resonant circuit and power amplifier. Feld discloses LCR series resonant circuit (fig.5, Ls Cs GL) and the LC parallel resonant circuit (fig. 5). It would have been obvious to one of ordinary skill in the art at the time the invention was

made to have the above limitation of Feld for impedance matching. Shohara disclosed a wireless communication apparatus comprising a low noise amplifier configured to amplify a voltage of a received signal (parag. 0034), a down-converter (fig.1, item 14) configured to down-convert the voltage-amplified received signal by frequency conversion, an automatic gain controller (fig.1, item 28), an analog-digital converter (fig.1, item 18), digital- analog converter (fig.1, item 44) which converts transmit data to an analog signal, an up-converter (fig.1, item 48) configured to up- convert the analog transmit signal by frequency conversion, a power amplifier (parag.0034) configured to amplify power of the up-converted transmit signal, and a signal processing circuit (fig.1, item 50) configured to perform digital signal processing of transmit/receive data.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to have all this limitation for a design choice.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art henceforth "Admission" and further in view of Kasuga (patent No.: US 4524422)

With respect to claim 14:

Admission discloses an amplifier comprising: an amplification device (fig.8, item 102), an output terminal of the amplification device being an output terminal of the amplifier (fig.8, item 102) and a band pass filter connected in parallel to the output terminal of the amplification device (fig.8). Admission did not disclose s-plane in which the plurality of pole is provided and zero are provided between the poles. Kasuga discloses a band pass filter with s-plane in which the plurality of pole is provided and zero are provided

between the poles (col.2, lines 54-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have s-plane in which the plurality of pole is provided and zero are provided between the poles simply for design choice.

9. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art henceforth "Admission" and further in view of Feld (Patent No.: US 6281755B1) and Kasuga (patent No.: US 4524422) and Daners (Patent No.: US 6229393B1).

With respect to claims 15 and 16:

The rejection of claim 14 is incorporated; Admission, Feld and Kasuga did not disclose capacitor and inductance not in series between an output terminal of the amplifier device and output terminal of amplifier. Daners disclosed capacitor and inductance not in series between an output terminal of the amplification device and output terminal of amplifier (fig.1b). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a capacitor and inductance not in series between an output terminal of the amplifier device and output terminal of amplifier for a design purpose.

10. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art henceforth "Admission" and further in view of Kasuga (patent No.: US 4524422) and Shohara (Pub. No.: US 2005/0078743A1).

With respect to claim 19:

Admission discloses an amplifier comprising: an amplification device (fig.8, item 102), an output terminal of the amplification device being an output terminal of the amplifier (fig.8, item 102) and a band pass filter connected in parallel to the output terminal of the amplification device (fig.8). Admission did not disclose plurality of poles provided on a left side of an s-plane and a plurality of zeros arranged between the poles, at least two zeros being arranged at locations other than an origin of the s-plane; a down-converter configured to down-convert the voltage-amplified received signal by frequency conversion; an automatic gain controller; an analog-digital converter; and a signal processing circuit configured to perform digital signal processing of received data. Kasuga discloses a band pass filter with s-plane in which the plurality of pole is provided and zero are provided between the poles (col.2, lines 54-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have s-plane in which the plurality of pole is provided and zero are provided between the poles simply for design choice. Shohara disclosed a wireless communication apparatus comprising a low noise amplifier configured to amplify a voltage of a received signal (parag. 0034), a down-converter (fig.1, item 14) configured to down-convert the voltage-amplified received signal by frequency conversion, an automatic gain controller (fig.1, item 28), an analog-digital converter (fig.1, item 18), and a signal processing circuit configured to perform digital signal processing of received data (fig.1, item 50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have all this limitation for a design choice.

With respect to claim 20:

Admission discloses an amplifier comprising: an amplification device (fig.8, item 102), an output terminal of the amplification device being an output terminal of the amplifier (fig.8, item 102) and a band pass filter connected in parallel to the output terminal of the amplification device (fig.8). Admission did not disclose plurality of poles provided on a left side of an s-plane and a plurality of zeros arranged between the poles, at least two zeros being arranged at locations other than an origin of the s-plane; a down-converter configured to down-convert the voltage-amplified received signal by frequency conversion; an automatic gain controller; an analog-digital converter; and a signal processing circuit configured to perform digital signal processing of received data. Kasuga discloses a band pass filter with s-plane in which the plurality of pole is provided and zero are provided between the poles (col.2, lines 54-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have s-plane in which the plurality of pole is provided and zero are provided between the poles simply for design choice. Shohara disclosed a wireless communication apparatus comprising a low noise amplifier configured to amplify a voltage of a received signal (parag. 0034), a down-converter (fig.1, item 14) configured to down-convert the voltage-amplified received signal by frequency conversion, an automatic gain controller (fig.1, item 28), an analog-digital converter (fig.1, item 18), digital- analog converter (fig.1, item 44) which converts transmit data to an analog signal, an up-converter (fig.1, item 48) configured to up- convert the analog transmit signal by frequency conversion, a power amplifier (parag.0034) configured to amplify power of the up-converted transmit

signal, and a signal processing circuit (fig.1, item 50) configured to perform digital signal processing of transmit/receive data. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have all this limitation for a design choice.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJIBOLA AKINYEMI whose telephone number is (571)270-1846. The examiner can normally be reached on monday- friday (8.30-5pm) Est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, YUWEN PAN can be reached on (571) 272-7855. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA
/Yuwen Pan/
Primary Examiner, Art Unit 2618